ALIGNED CLOCK FORWARDING SCHEME

FIELD OF THE INVENTION

[0001]   The present invention generally relates to the design of an electronic system, and more specifically to the design of the clock scheme in a computer or electronic system.

BACKGROUND OF THE INVENTION

[0002]   In an electronic system, subsystems communicate with one another by transferring data among them in order to maintain the normal operation of the whole system. Almost all the modern electronic systems have sequential circuits that require an input clock for these systems to function properly. The source of the input clock for each subsystem may or may not be the same.

[0003]   When data or a signal is transmitted from one subsystem to another subsystem, the transferred signal and the input clock entering the receiving subsystem usually have to comply with some requirements in timing. For example, these signals must be aligned when they arrive at the receiving subsystem. The relationship in timing is specified in the datasheet of various subsystems such as DRAM specification or PCI bus specification.

[0004]   With reference to FIG. 1, a conventional electronic system with two subsystems is illustrated. A clock generator 100 provides clock inputs CK1 and CK2 to a first subsystem 101 and a second subsystem 102 respectively. As shown in FIG. 1, the two clock inputs CK1 and CK2 have different paths in the system. In the electronic system, data are transferred from the first subsystem 101 to the second subsystem 102.

[0005]   Because of the path difference, some environmental factors may affect the timing relationship between CK1 and CK2. For example, the trace length of the clock input CK1 to the first subsystem 101 may be longer than the trace length of the clock input CK2. The signal driving capability of the first subsystem 101 can also be different from that of the clock generator 100, and the leaving time of the clock input from the clock generator 100 may be different from that of the data sent from the first subsystem 101 to the second subsystem 102. Consequently, CK1 has a clock skew with respect to CK2 as illustrated in FIG. 2. When the second subsystem samples the transferred data, incorrect data may be received as a result of the skew.

[0006]   In general, there are two important timing requirements to be met in the clock and data signals of an electronic system. One is setup time and the other is hold time. Two possible data transactions with output delays are shown in FIG. 2, i.e., Data with output delay I and Data with output delay II, respectively. While one meets both setup and hold time requirement, the other violates the timing requirement.

[0007]   How to satisfy the timing requirement plays an important role in designing modern electronic systems. In a computer system, increasing operation frequency is an effective approach to providing more operation power and higher performance. As the higher operation frequency is used and a cycle time is shortened, it becomes more and more difficult to meet the AC conditions of signals transferred among the computer subsystems. The timing relationship between the input clock and the transferred data is one of the AC conditions that have to be satisfied.

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SUMMARY OF THE INVENTION

[0008] This invention has been made to meet the above-mentioned requirement in timing relationship of signals and clocks in a computer or electronic system. The primary object of this invention is to provide a clock scheme so that the timing relationship between clocks and data or signals in a system having multiple subsystems can be well controlled.

[0009] Accordingly, an aligned clock forwarding scheme is provided in this invention to maintain the timing relationship between an input clock and a transferred data signal. Within a first subsystem, the aligned forwarding scheme includes a first circuit path generating an aligned clock output signal sent to a second subsystem and a second circuit path generating an aligned data signal to the second subsystem. An external clock input serves as the clock signal for the aligned clock forwarding scheme.

[0010] The two circuit paths have identical circuit components so that they have the same physical characteristics. Each circuit path comprises a D flip-flop and an output buffer. A clock multiplication circuit receives the external clock input and generates multiplied clock signals to control the D flip-flops of both first and second circuit paths. Both clock output and data signal experience the same environmental effect to avoid any additional skew. An inverter may also be used to generate a clock output with an inverse phase if necessary.

[0011] The foregoing and other objects, features, aspects and advantages of the present invention will become better understood from a careful reading of a detailed description provided herein below with appropriate reference to the accompanying drawings.

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BRIEF DESCRIPTION OF THE DRAWINGS

[0012]   FIG. 1 shows a conventional electronic system in which the clock inputs of two subsystems are provided by the same clock generator.

[0013]   FIG. 2 shows the timing relationships between the transferred data and the clock signals of the subsystems in the conventional system shown in FIG. 1.

[0014]   FIG. 3 shows an electronic system designed with the aligned clock forwarding scheme according to the present invention.

[0015]   FIG. 4 shows a simplified circuit diagram for the aligned clock forwarding scheme in which the internal data paths of data and aligned clock have mirrored structures inside the subsystem.

[0016]   FIG. 5 shows the timing relationships between the transferred data and clock signals of the circuit diagram shown in FIG. 4.

[0017]   FIG. 6 shows an alternative simplified circuit diagram for the aligned clock forwarding scheme in which an inverse-phase clock is generated with an additional inverter.

[0018]   FIG. 7 shows the timing relationships between the transferred data and clock signals of the circuit diagram shown in FIG. 6.

[0019]   FIG. 8 shows an embodiment of the aligned clock forwarding scheme applied to the memory control scheme in a personal computer system based on the present invention.

[0020]   FIG. 9 shows the timing diagram of the embodiment in FIG. 8, which effectively maintains the precise and accurate timing relationship with the aligned clock

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forwarding scheme of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0021]   With reference to FIG. 3 , the present invention provides an aligned clock forwarding scheme to overcome the problem associated with the timing difference of input clocks in different subsystems of an electronic system. A clock generator 300 provides a clock input CK1 to a first subsystem 301. The first subsystem 301 then provides a clock input CK2 to the second subsystem 302. In the electronic system, data is also transferred from the first subsystem 301 to the second subsystem 302. The clock input CK2 and the data are properly aligned so as to meet the timing specification.

[0022]   FIG. 4 shows a simplified circuit diagram for implementing the aligned clock forwarding scheme according to this invention. As can be seen, the output paths of both data and CK2 are identical. The output path comprises a D flip-flop 401 and an output buffer 402. In this scheme, both trace length and driving capability for the clock input CK2 and the data to the second subsystem 302 are the same. Therefore, the leaving time of the clock input and data signals can be well controlled. The simplified circuit also comprises a clock multiplication circuit for generating multiplied clock signals to control the D flip-flops in the output paths of both data and CK2. The clock multiplication circuit includes a clock multiplier 403 and an inverter 404 as shown in FIG. 4.

[0023]   The flip-flop delay, output buffer delay and trace length of the clock input and data are the same and mirrored as one architecture shown in FIG. 4. The timing relationship between the clock input CK2 and data is shown in FIG. 5. With the aligned clock forwarding scheme shown in FIG. 4, the timing can be well maintained and the

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setup time violation can be effectively eliminated. However, the hold time violation may still occur under this architecture as illustrated in FIG. 5. Two possible data transactions with output delays are shown, i.e., Data with output delay I and Data with output delay II, respectively. Although the setup time requirement is met, both of them violate the hold time requirement.

[0024]   FIG. 6 shows another simplified diagram for the aligned clock forwarding scheme according to this invention. In some case, it is desirable to generate a clock input with an inverse phase by using an additional inverter 603 as illustrated in FIG. 6. FIG. 7 shows the timing relationships between the transferred data and the clock signals corresponding to the circuit of FIG. 6. Two possible data transactions with output delays are shown, i.e., Data with output delay I and Data with output delay II, respectively. Both of them meet the setup and hold time timing requirement as shown in FIG. 7.

[0025]   In the simplified circuit, the external clock signal is inverted by an inverter 602 before entering the output path of CK2. The circuit also comprises a clock multiplication circuit for generating multiplied clock signals to control the D flip-flops in the output paths of both data and CK2. The clock multiplication circuit includes a clock multiplier 604 which receives the external clock signal and sends a multiplied clock signal to the D flip-flop in the output path of the data. The inverter 603 receives the multiplied clock signal and sends an inverted multiplied clock signal to the D flip-flop in the output path of CK2.

[0026]   With reference to FIG. 8, an aligned clock forwarding scheme of this invention is applied to a clock scheme of a memory control circuit. The architecture implemented in the aligned clock forwarding scheme is based on the FIG. 6 in which an

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inverse-phase clock is generated with an additional inverter. The timing relationship of the embodiment is shown in FIG. 9.

[0027]   There are four output paths in the circuit of FIG. 8. The first output path generates a clock signal CK2, the second output path generates a data strobe signal, the third output path generates a 2X data signal and the fourth output path generates a 1X data signal. Each output path has a D flip-flop and an output buffer. An inverter 801 receives an external clock signal and sends an inverted clock signal to the first output path.

[0028]   A clock multiplication circuit is used to generate multiplied clock signals for clocking the D flip-flops in the four output paths. The clock multiplication circuit includes a clock multiplier 804 which sends the multiplied clock signals to the D flip-flops in the third and fourth output paths. The inverter 802 inverts the multiplied clock signal and sends an inverted multiplied clock signal to the D flip-flop in the first output path. Similarly, another inverter 803 inverts the multiplied clock signal and sends an inverted multiplied clock signal to the D flip-flop in the second output path.

[0029]   Based on the inverse-phase clock generated architecture, the Data 2X Strobe signal can be in phase with the new CK2 signal. In this manner, the Data 2X signal can be well controlled and maintained with the Strobe and Data center aligned in accordance with the timing requirement. The Data 1X can be well controlled as it has been shown in FIG.7. The processing rate of the Data 2X signal is twice of the Data 1X signal, and the cooperation of Data 1X and Data 2X leads to high speed processing in the embodiment by using the present invention.

[0030]   In summary, the signal paths of a data signal and a clock input according to

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the aligned clock forwarding scheme have the same physical characteristics such as output capacitance, resistance, inductance on a package and trace length on a board. Therefore, even if there are environmental changes such as voltage and temperature variation, both clock input and data signal experience the same effect. There is no additional skew between the two signals during the data transfer between two subsystems.

[0031]   Although the present invention has been described with reference to the preferred embodiments, it will be understood that the invention is not limited to the details described thereof. Various substitutions and modifications have been suggested in the foregoing description, and others will occur to those of ordinary skill in the art. Therefore, all such substitutions and modifications are intended to be embraced within the scope of the invention as defined in the appended claims.